



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,233	01/16/2002	Robert E. Stengel	CM03359J	6380

7590 10/05/2005  
Andrew S. Fuller  
Motorola, Inc.  
Law Department  
8000 West Sunrise Boulevard  
Fort Lauderdale, FL 33322

EXAMINER

WONG, LINDA

ART UNIT	PAPER NUMBER
----------	--------------

2634

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/050,233	<b>Applicant(s)</b> STENGEL ET AL.	
	<b>Examiner</b> Linda Wong	<b>Art Unit</b> 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 3-5, 8-11, 13-15, 17-19, 34, 36-40, 42-49, 52-60, 71, 73 and 75-80 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-10, 79 and 80 is/are allowed.
- 6) ☒ Claim(s) 3-5, 11, 13-15, 17-19, 34, 40, 49, 52-56, 59 and 60 is/are rejected.
- 7) ☒ Claim(s) 36-39, 42-48, 57, 58, 71, 73 and 75-78 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Response to Amendment***

1. Due to the applicant's amendments, see Amendment after Non-Final, filed 7/20/2005, the objection(s) of claim(s) 7-9 have been withdrawn.
2. Due to the applicant's amendments, see Amendment after Non-Final, filed 7/20/2005, the 35 USC 112 rejections of claims 11 and 15 have been withdrawn.

***Claim Objections***

3. **Claim 38** is dependent on claim 35, but claim 35 has been cancelled. The new independent claim is claim 34.
4. **Claim 71** objected to under 37 CFR 1.75 as being a substantial duplicate of claim 73. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Claim Rejections - 35 USC § 112***

5. **Claims 11,15,34,40,49** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2634

- a. **Claims 11,15,34,40** recite the limitation of "... a tap selection circuit that selects a first sequence of tap addresses Cja; ...". The tap selection circuit does not show a clear connection between the delay locked loop outputting a plurality of addressable tap outputs and the tap selection circuit and the inputs and outputs of the tap selection circuit. For example, as recited in claim 8, "the first tap selection circuit that produces a first set of tap addresses to select a first set of the plurality of tap outputs from the delay line ..". Claim 8 clearly recites the first tap selection chooses tap addresses from the outputs of the delay line and outputs a first set of tap addresses. Such a recitation should also be included in claim 11 to show the connection between the delay line and the tap selection circuit.
- b. **Claim 49** recites the limitations "... selecting a first sequence of the tap outputs according to a first timing to produce a first output signal Fout1; selecting a second sequence of the tap outputs according to a second timing to produce a second output signal Fout2; ..." The tap selections should clearly recite the selecting the tap outputs produced from the delay line so as to clearly state what the inputs and outputs are from the selection.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2634

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 3-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bockelman<sub>1</sub> (US Publication No.: 20020110211) in view of Nakase et al. (US Publication No.: 20020059352).

a. **Claims 3-5** are rejected as stated in the previous action. Please refer to the rejection of claims 1 and 2. Due to the amendments to claims 3-5, claims 1 and 2, as recited in the claimed set, did not recite the limitation of frequency, phase and amplitude modulating the first output signal with the second output signal. Nakase et al discloses a delay line which delays the input string in terms of the frequency. Thus, the first input signal is frequency modulated with the second input signal. It would be obvious to one skilled in the art, based on design choice, to phase and amplitude modulate by using a delay line for delaying the input signal by the phase or amplitude, wherein modulating the first output with the second output would produce a phase or amplitude, respectively, modulated output.

b. **Note: The following rejections are rejections to claims 1 and 2 as stated in the previous office action. Due to the amendments, claims 3-5 have been revised to incorporate claims 1 and 2 as was previously claimed.**

i. **Claim 1**, Bockelman<sub>1</sub> discloses a delay locked loop comprising a plurality of tap outputs (Fig. 2, labels 38, 46, 48, 36, and 16), a first and second selection circuit

comprised of producing first and second set of tap addresses (Fig. 8, output from label 20, output from label 60 and pg. 2, paragraph [0019], lines 8-9) to select a first and second set of plurality of tap outputs from a delay line (Fig. 8, labels 16, 18, 56 and 58) to produce a first and second output signal (Fig. 8, output from label 18 and 58). Although Bockelman<sub>1</sub> does not disclose two timings used for the selection of a plurality of tap outputs from a delay line, Nakase et al. discloses a delay line with two selections based on timings. (Fig. 1, labels clk 2, 20 and 21) It would be obvious to one skilled in the art to apply the use of timings disclosed by Nakase et al to Bockelman<sub>1</sub>'s process of outputting phase shifts of a clock signal to produce different tap addresses at different timings, providing outputs with different shifts.

- ii. **Claim 2**, Although Bockelman<sub>1</sub> does not disclose a modulator, Nakase et al disclose a modulator combining the first and second output signals to produce a modulated signal. (Fig. 1, output from labels 30, 31, 32, 40 and output L3) As explained in the specification of the applicant and recited in this claim, in Fig. 10 the modulated signal is produced by combining the outputs from the first and second selection circuit. Thus, although Nakase et al does not explicitly disclose that the output L3 as a modulated signal, based on the description provided by the applicant, Nakase et al's output is equal to the modulated signal disclosed by the applicant.

### ***Claim Rejections - 35 USC § 102***

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 7. **Claim 49** is rejected under 35 U.S.C. 102(e) as being anticipated by Nakase et al (US Publication No.: 20020059352).
  - a. **Claim 49**, Nakase et al discloses a delay line output a plurality of tap outputs (Fig. 1, labels D0-D7), selecting a first sequence of tap outputs to a first timing to produce a first output signal Fout1 using a first

multiplexor (Fig. 1, labels 20,8,Clk2) and selecting a second sequence of tap outputs to a second timing to produce a second output signal Fout2 using a second multiplexor (Fig. 1, labels 21,8, and Clk1). Although Nakase et al does not explicitly state applying the addresses of the first and second sequence of outputs, Nakase et al shows in Fig. 1, the points or addresses of the delay taps as the inputs to the selector.

8. **Claims 11,13-14,15,17-19,52-55,56,59-60** are rejected under 35

U.S.C. 102(e) as being anticipated by Juan et al (US Publication No.: 20030099321).

- a. **Claim 11**, Juan et al discloses a delay locked loop comprising a delay line (Fig. 7, labels 24,56,60), a tap selection circuit for selecting a first sequence of addressable taps (Fig. 7, labels 250 and 24), an adder for adding the amount of phase error detected to the delays to generate a second set of tap addresses (Fig. 11, labels 518, 310 and 350, Fig. 7, labels 280, 270, 274 and page 8, paragraphs [0105] and [0106]) and a first and second multiplexor, wherein the first set of taps are applied to the first mux and the second set of taps are applied to the second mux (Fig. 7, labels 24,250,270,274), outputs Fouta and Foutb (Fig. 7, outputs from labels 250 and 212), wherein Fouta and Foutb differ by a desired phase. (page 8, paragraphs [0105] and [0106])
- b. **Claims 13 and 14**, Juan et al discloses shifting the delay lines based on the phase error, thus the phase shift can comprise a variable time shift or

a 90 degree shift or a fixed shift, depending on the amount of phase error is found. (Fig. 11, Fig. 7 and page 8, paragraphs [0105] and [0106])

- c. **Claim 15** inherits all the limitations of claim 11 but claim 11 does not recite the first and second multiplexors each comprising N:1 multiplexors having N inputs. Juan et al discloses such a limitation in Fig. 7, labels 250 and 274)
- d. **Claims 17, 18 and 19** inherit the limitations of claims 13 and 14.
- e. **Claim 52**, Juan et al discloses a delay locked loop comprising a delay line with a plurality of addressable tap outputs (Fig. 6, labels 24, 56 and 60), selecting a first sequence of tap address (Fig. 7, label 250), detecting the phase shift using a phase detector or global average tuning to add or adjust the amount of adjustments needed to adjust the delays of the taps. (Fig. 11, and page 8, paragraphs [0105] and [0106])
- f. **Claim 53**, Juan et al discloses applying the first sequence of tap address to a first multiplexor (Fig. 7, labels 250 and 24) and applying the second sequence of tap address to a second multiplier (Fig. 7, labels 270 and 274). Although Juan et al does not explicitly state the outputs from the first and second multiplexor differ by a phase shift, Juan et al discloses adjusting the delays of the delay line based on the tuning the delay line based on the phase. Thus, Juan et al, inherently, discloses a first and second output from the multiplexor as having outputs differing by a phase shift. (Fig. 11, Fig. 7 and page 8, paragraphs [0105] and [0106])

Art Unit: 2634

- g. **Claims 54 and 55**, Juan et al discloses shifting the delay lines based on the phase error, thus the phase shift can comprise a variable time shift or a 90 degree shift, depending on the amount of phase error is found. (Fig. 11, Fig. 7 and page 8, paragraphs [0105] and [0106])
- h. **Claim 56** inherits all the limitations of claims 52,53,54 and 55.
- i. **Claims 59 and 60** inherit all the limitations of claims 54 and 55.

### ***Allowable Subject Matter***

- 9. **Claims 8,9-10,79-80** are allowed over prior art.
  - 10. **Claims 34,40** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
  - 11. **Claims 71 and 73** would be allowable if rewritten or amended to overcome the objection set forth in this Office action.
  - 12. **Claims 36-39, 42-48,57-58,75-78** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- Claim 9 must be rewritten to overcome all objections.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The

Art Unit: 2634

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong



STEPHEN CHIN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600